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<td></td>
</tr>
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</tr>
</tbody>
</table>
INTRODUCTION
Scope of the Report

- This report provides a detailed picture of the patent landscape for TSV Stacked Memory, with 3-dimensional structure.
- This report covers patents published worldwide up to June 2016.
- We have selected and analyzed more than 1,500 patents split in more than 400 patent families relevant to the scope of this report.

Included in the report

- Any patent describing a **3D stacked memory using TSV** (Through Silicon Via).
- Patents mentioning **package** of these TSV memory dies or chips.

Not included in the report

- Patents with stacked memory **without TSV** (Through Silicon Via).
- Patents with memory that are **not in a 3-dimensional structure**.
- Patents with stacked memory **used in a device**.
- Patents with stacked memory **using wire connection**.
METHODOLOGY

• The data were extracted from the FamPat worldwide database (Questel-ORBIT) which provides 80+ million patent documents in 95 offices.

• The search for patent was performed in June 2016 hence patents published after this date will not be available in this report.

• The patents were grouped by patent family. A patent family is a set of patents filed in multiple countries to protect a single invention by a common inventor(s). A first application is made in one country – the priority country – and is then extended to other countries.

• The selection of the patents has been done both automatically and manually (all details in next slides).

Number of selected patent families for the TSV Stacked Memory Patent Landscape Analysis:
417 over a number of returned results > 4,000

• The statistical analysis was performed with Orbit IP Business Intelligence web based patent analysis software from Questel.

• The patents were manually categorized in technical segments using keyword analysis of patent title, abstract and claims, in conjunction with expert review of the subject-matter of inventions (all details in next slides).

• For legal status of European (EP) and PCT (WO) patent applications, EPO Register Plus has been used. For legal status of US patents, USPTO PAIR has been used. For legal status of other patents, information have been gotten from their respective national registers.
**METHODOLOGY**


**Phase I**
- Keywords and term-set definition
- Search equations / Search strategy

**Phase II**
- Manual screening of the results
- Patent classification
  - Relevant
  - Non relevant
- Refine search using IPC classes and citations analysis

**Phase III**
- Patent Segmentation
  - Segmentation improved during patent analysis
- Patent Analysis
  - Landscape Overview
  - In-depth analysis of Key Technology Segments and Key Players
  - Patent Ranking and Key Patents analysis
### METHODOLOGY

#### Search Equations

<table>
<thead>
<tr>
<th>STEP</th>
<th>SEARCH EQUATION</th>
<th>RESULT</th>
</tr>
</thead>
</table>
| Patents related to Memory | **Step-1**
| Patents related to TSV Memory | **Step-2**
| | **Step-1** AND ((THROUGH 1D (SILICON? OR SUBSTRATE? OR WAFER? OR GLASS+ 1D (VIA? OR HOLE? OR INTERCONNECT+)) OR (THROUGH 0W HOLE 0W (VIA? OR HOLE? OR INTERCONNECT+)) OR (THROUGH 0W VIA 0W (HOLE? OR INTERCONNECT+)) OR ((THROUGH 0W WIRE) 0W INTERCONNECT+) OR TSV? OR TSV-BASED)/BI/CLMS | >800 |
| Patents related to Memory Manufacturing Process | **Step-3**
| | **Step-1** AND (MICRO_BUMP? OR MICRO_PADS OR FLIP_CHIP+ OR COPPER PILLAR? OR CU PILLAR? OR CU-CU OR INTERPOSERS OR TRANSPOSER? OR UNDER_FILL+ OR (((CARRIER+ OR HOST+ OR HANDL+ OR SUPPORT+ OR BOND+) 2D (TEMPO+ OR PROVISIO+ OR GLASS)) OR (BONDING OR DE_BONDING)) 2D (PACKAGE? OR DIE? OR CHIP?) OR ((THIN+ OR SLIM+ OR CMP OR POLISH+ OR GRIND+) 2D (WAFER? OR SUBSTRATE?)))| >3,000 |
| Patents related to Memory Stacking | **Step-4**
| | **Step-1 AND Step-2/DESC AND (+stack+ OR pile OR piled OR piling OR pile_up))/BI/CLMS | >1,000 |
| Automatically and manually selection | **Step-5**
| | Step-2 OR Step-3 OR Step-4 | >4,300 |

Relevant patent families selected for the study

417
METHODOLOGY

Segmentation of Patents

Patents selected for the study were manually categorized into following segments.

- 3D TSV Stacked Memory
  - TSV: 64 patent families
  - Bumping: 27 patent families
  - Stacking: 156 patent families
  - Package: 77 patent families
  - Others (System, Method, …): 118 patent families

417 patent families
TECHNOLOGY OVERVIEW

3D Integration Memory

The 3D approach can be done at two levels:

• **Front-end (silicon) approach:** Memory cells are vertically organized, not horizontally. Monolithic 3D wafers are manufactured all in one fab, and rather than stacking 2 or more wafers, a base wafer is used onto which additional layers of crystallized silicon and metalized layers are added using traditional fab equipment. This approach is used for 3D NAND (also called VNAND by Samsung), and is not possible with DRAM.

• **Back-end (packaging) approach:** Memory chips are stacked and connected with 3D assembly technologies like TSV (through silicon vias). 3D TSVs involve taking two finished device wafers (either from the same or different fabs) and vertically interconnecting them at the chip level with through silicon vias (TSVs) in either wafer-to-wafer or die-to-wafer processes. This approach is used for DRAM with HMC and HBM techniques.
3D packaging Through Silicon Via (TSV) approach is used in different offers (DDR4, Wide IO, HBM, HMC) in order to increase bandwidth and bit density. Those offers get from low-end applications like networks servers (DDR4) up to high-end computing applications (HMC, HBM).

**Bandwidth is the most important challenge of DRAM**

Micron is working on HMC with Intel

SK Hynix released HBM1 with AMD

SK Hynix, Samsung are working on HBM2

SK Hynix released Wide I/O2

Samsung and SK Hynix released DDR4 with TSVs
**PATENT LANDSCAPE ANALYSIS**

**Time Evolution of Patent Publications**

**TSV Stacked Memory IP Dynamics**

400+ patent families comprising 1,500+ patents

<table>
<thead>
<tr>
<th>Year</th>
<th>IBM USXXXXX</th>
<th>Samsung</th>
<th>SK Hynix</th>
</tr>
</thead>
<tbody>
<tr>
<td>1990</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1991</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1992</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1993</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1994</td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1995</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1996</td>
<td>1</td>
<td></td>
<td></td>
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<td>1997</td>
<td>1</td>
<td></td>
<td></td>
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<tr>
<td>1998</td>
<td>2</td>
<td></td>
<td></td>
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<tr>
<td>1999</td>
<td>4</td>
<td></td>
<td></td>
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<td>2000</td>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2001</td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2002</td>
<td>4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2003</td>
<td>4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2004</td>
<td>12</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2005</td>
<td>7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2006</td>
<td>16</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2007</td>
<td>25</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2008</td>
<td>16</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2009</td>
<td>44</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2010</td>
<td>52</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2011</td>
<td>57</td>
<td></td>
<td></td>
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<tr>
<td>2012</td>
<td>53</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2013</td>
<td>40</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2014</td>
<td>42</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2015</td>
<td>14</td>
<td></td>
<td></td>
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<tr>
<td>2016</td>
<td>14</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Earliest Publication Year of Each Patent Family**

- **IBM USXXXXX**
- Three-dimensional memory card structure with internal direct chip attachment

**CAGR 2005-2012**

- 6.4%

**Expected patent publications in 2016**

**Note:** The patent search was done in June 2016, thus the data corresponding to the year 2016 are not complete. At the time of the patent search, 14 patent families had been published in 2016.

- First patents involving TSV stacked memories were already published in the 1990s (USXXXXX, IBM), but the development of the technology really started in the mid-2000s with a significant increase of patent publications since then.
- To this date, more than 400 patent families relating to TSV stacked memory technology have been published. We observed a decrease of patent applications the last two years, while the first products appeared on the market (Wide I/O, HBM, DDR4 ...).
• Assignee XX has a patent portfolio mainly focused on Korea and USA with 24 and 69 patented inventions in force respectively.
• Among the main assignees, Assignee XX shows the most worldwide IP strategy with a lot of granted patents in all geographic areas. Assignee XX patent portfolio has the strongest position in the map of granted patents.
• Assignees XX have no enforceable patents in the European area.
PATENT LANDSCAPE ANALYSIS
Summary of Assignees’s Patent Portfolio

- The top-6 of the main patent assignees owns more than 80% of the whole patent families, with most portfolios including more than 40 families each.
- The IP leaders are XX and XX. XX holds the largest patent portfolio in the TSV Stacked Memory with 117 patent families (comprising 539 patents) thanks to the acquisition of XX in 2013. XX has a worldwide IP strategy and should improve its presence in Europe in the next years.
- XX owns over 80% of alive patents (138 granted patents and 99 pending patent applications) and is strongly active in the USA and Korea. With 109 patent families (comprising 280 patents), XX holds the 2nd largest portfolio in the domain.

<table>
<thead>
<tr>
<th>Patent Applicants</th>
<th>No. of patent families</th>
<th>Oldest priority date of the portfolio (average)</th>
<th>No. of patent families filed / year</th>
<th>No. of patent members (average)</th>
<th>Patent average age (year)</th>
<th>% of granted patents</th>
<th>% of pending patent applications</th>
<th>% of dead patents (rejected, lapsed, expired)</th>
<th>No. of alive patents / Family (granted, pending)</th>
<th>No. of granted patented by country</th>
</tr>
</thead>
<tbody>
<tr>
<td>COMPANY XX</td>
<td>XX</td>
<td>20XX</td>
<td>XX</td>
<td>XX</td>
<td>4</td>
<td>XX%</td>
<td>XX%</td>
<td>XX%</td>
<td>XX</td>
<td>US 69 - EP 7 - JP 6 - CN 3 - TW 24</td>
</tr>
<tr>
<td>COMPANY XX</td>
<td>XX</td>
<td>20XX</td>
<td>XX</td>
<td>XX</td>
<td>XX%</td>
<td>36%</td>
<td>XX%</td>
<td>XX%</td>
<td>XX</td>
<td>US 43 - EP 5 - JP 11 - CN 2 - TW 15</td>
</tr>
<tr>
<td>COMPANY XX</td>
<td>63</td>
<td>19XX</td>
<td>XX</td>
<td>337</td>
<td>XX</td>
<td>XX%</td>
<td>XX%</td>
<td>XX%</td>
<td>XX</td>
<td>US 44 - EP 8 - JP 15 - CN 20 - TW 23 - KR 18</td>
</tr>
<tr>
<td>COMPANY XX</td>
<td>XX</td>
<td>20XX</td>
<td>XX</td>
<td>4.2</td>
<td>XX%</td>
<td>XX%</td>
<td>XX%</td>
<td>XX%</td>
<td>19%</td>
<td>US 47 - EP 33 - JP 9 - CN 2 - TW 2</td>
</tr>
<tr>
<td>COMPANY XX</td>
<td>XX</td>
<td>20XX</td>
<td>XX</td>
<td>5.2</td>
<td>XX%</td>
<td>XX%</td>
<td>XX%</td>
<td>XX%</td>
<td>5.0</td>
<td>US 33 - EP 10 - JP 5 - CN 20 - TW 13</td>
</tr>
<tr>
<td>COMPANY XX</td>
<td>XX</td>
<td>19XX</td>
<td>XX</td>
<td>XX</td>
<td>46%</td>
<td>XX%</td>
<td>XX%</td>
<td>XX%</td>
<td>XX%</td>
<td>US 7 - EP 6 - JP 4 - CN 3 - TW 1</td>
</tr>
</tbody>
</table>

**highest value in column**  **lowest value in column**
• **XX** shows a strong IP leadership. The company combines a high number of granted patents with a lot of pending patent applications.

• **XX and XX** have a significant leadership. Both own a large granted patent portfolio and are still active in terms of patent filings.

• **XX** could see its IP leadership increase in the future, considering their current patenting activity.
Key Player XX

Patent Portfolio Overview

197 patents within 68 patent families on TSV Stacked Memory

- Patent publications in 2008 rely on chip stack structure with through-silicon vias, in order to overcome the problems caused in the stack package using the metal wires, prevent the electrical characteristics of the stack package from deteriorating and enable miniaturization of the stack package. They describe solutions to absorb thermally-induced stresses, prevent warpage and cracks and improve operation.
- XX enters production in end 2000s and joined in 2011 YY program.
- In 2011-2015, XX was actively working on different kind of solutions: heat dissipation, adhesion, error failure,... in the memory stack.
- XX doesn’t have a worldwide IP strategy in 3D TSV Memory. Indeed, XX has no alive patents in Europe and very few granted patents in Japan and Taiwan. However the high number of pending patent applications in Taiwan, but also Korea, China or USA will increase the number of granted patents in these countries in the future. XX has strong IP presence in USA.
The package structure includes 4 stacked dies, TSV & microbumps for die connection, flip chip bumps for package connection.

A stacked memory device includes a plurality of a plurality of memory chips; a first path to transmit a command signal to at least one of the plurality of memory chips; and a second path coupled to the plurality of memory chips, the second path to transmit a refresh control signal for controlling a refresh operation of at least one of the plurality of memory chips.

**US2013XXXXXX (2013)**
A chip stack package where a plurality of through silicon vias are efficiently and readily aligned and a capacitance of a signal path is efficiently and readily adjusted.
<table>
<thead>
<tr>
<th>Key Patent Families</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>KEY PATENT FAMILIES</strong></td>
</tr>
<tr>
<td>Patent number (representative member), earliest publication date, title and principal drawing</td>
</tr>
<tr>
<td><strong>RATIONALES FOR CHOICE</strong></td>
</tr>
<tr>
<td>Refer to slide 18 for selection criteria</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Patent Number</th>
<th>Title and Principal Drawing</th>
<th>Rationales for Choice</th>
</tr>
</thead>
<tbody>
<tr>
<td>USXXXXXX (2002)</td>
<td>Method and apparatus for generating a device id for stacked devices</td>
<td>- Future memory devices may utilize new technologies in packaging stacked devices, such as through-silicon vias or optical technology. The conventional method of bonding out a unique device ID for each stacked device, as described above, may not be practical for future device stacking technologies. - The present invention provides a method and apparatus for generating a unique device identifier (device ID) for each addressable integrated circuit (IC) device in a multi-die package, such as a stacked-CSP (chip scale package). - More than 32 citations per year on average (mostly by TSMC) - 1 US granted patent, 40+ claims</td>
</tr>
<tr>
<td>USXXXXXX (2012)</td>
<td>Die-stacking using through-silicon vias on bumpless build-up layer substrates including embedded-dice, and processes of forming the same</td>
<td>- Disclosed embodiments relate to semiconductor microelectronic devices and processes of packaging them. - More than 7 citations per year on average (mostly by Micron Technology and Samsung Electronics) - Extended family (TW, US, CN, WO) - 3 granted patents (US, CN, TW), 40+ claims</td>
</tr>
<tr>
<td>USXXXXXX (2013)</td>
<td>3d interconnect structure comprising through-silicon vias combined with fine pitch backside metal redistribution lines fabricated using a dual damascene type approach</td>
<td>- Embodiments of the invention describe a 3D interconnect structure and process which combines through-silicon vias (TSVs) with very fine pitch backside metal redistribution layers (RDLs) using a dual damascene type process flow. This particular combination may allow for the physical locations of the TSVs to be decoupled from the chip-to-chip landing pad locations, thus providing greater circuit layout flexibility. In this manner multiple RDLs can be run between adjacent landing pad rows or columns. - Extended family (KR, US, CN, TW) - 2 granted patents (KR, US)</td>
</tr>
</tbody>
</table>
Key Player XX

Relevant Patented Technology

Use of thinner package substrates such as bumpless build-up layers in 3D integration schemes

Bumpless Build-Up Layer or BBUL is a processor packaging technology. It is bumpless since it does not use the usual tiny solder bumps to attach the silicon die to the processor package wires. It has build-up layers since it is grown or built-up around the silicon die. The usual way is to manufacture them separately and bond them together. Some semiconductor packages now use a coreless substrate, which does not include the thick resin core layer commonly found in conventional substrates.

A bumpless build-up layer (BBUL) is being formed to couple the TSV die 120 to the outside world. Although the BBUL is illustrated with the patterned first dielectric 129 and the second dielectric 136, it may be understood that several layers of metallization and dielectric can be used to form the BBUL, which ultimately is a coreless substrate with an embedded TSV die. Where the disclosed embodiments include BBUL technology on a coreless substrate, the several embodiments may be referred to as BBUL-C embodiments. Further because TSV dice are included the several embodiments may be referred to as TSV-die BBUL-C apparatus.

WOXXXXXXXX and WOXxxxxxxx (2012)
Multi-Channel Package
Solutions found in patents

A 2-channel semiconductor device with an 8-Gbit memory capacity may be implemented with two dies, not one die, thereby making it possible to prevent a decrease in density on a wafer and improving availability on edge dies. Similar implementations can be made with other sized memory capacity chips, such as two 16-Gbit chips combined into a 32-Gbit, 2-channel semiconductor package. As a result, an increase in production cost may be alleviated due to an increase in yield.

Each of the memory chips 3100, 3200, 3300, and 3400 is implemented with a multi-channel semiconductor device formed of two or more dies as described, thereby improving yield and reducing production cost.

The DRAM 4520 may be a DDR4 DRAM, and in one embodiment includes an interconnection part and is formed of two or more dies contained in a mono package, thereby improving yield of fabrication and making it possible to reduce production cost of the computing device.

The LPDDR4 package contains four connected dies. Each physical channel has two ranks of memory connected to it. This configuration requires the design team to extend the connection in a serial direction on each of the four channels on the package. Unfortunately, a 4-die package doesn’t provide 8-channel connectivity; there are only four channels of package balls on the 4-die package.

USXXXXXX, and USXXXXXXX (2016) Assignee XX

A memory device includes a plurality of channels 205, shown as eight channels, Channel 0 through Channel 7. In some embodiments, each channel includes a column or stack of tiles of memory strata.

The channel characteristics 300 include a requirement for an increasing number of pins for larger memory, such as the illustrated memories of density 8 Gb, 16 Gb, and 32 Gb. The division of memory into multiple channels requires command addressing at each channel, thus requiring a multiple of the pins required for a single channel of memory.

USXXXXXX (2014) Assignee XX
PATENT LITIGATIONS
ELM 3DS vs. SK Hynix

Case 1:14-cv-01432-UNA filed 21/11/2014
Plaintiff: ELM 3DS Innovation
Defendant: SK Hynix

Hynix has infringed and continues to infringe the Elm 3DS patents, by making, using, selling, offering for sale, importing, and/or selling in the United States, semiconductor products with multiple stacked dies, wherein the stacked dies are attached to silicon substrates with thin film patterns and used, sold, offered for sale, and/or imported into the United States, with knowledge of the Elm 3DS patents and in the infringement....

The Elm 3DS Patents in-suit in ELM 3DS vs. SK Hynix case disclose the invention of three-dimensional (3D) memory and semiconductor products that incorporate multiple stacked dies, wherein the stacked dies are attached to silicon substrates with thin film patterns and used, sold, offered for sale, and/or imported into the United States, with knowledge of the Elm 3DS patents and in the infringement....

The disclosed technology also improves memory density because multiple stacked dies can be placed on top of one another and electrically connected. The disclosed technology reduces the number of interconnects, resulting in a smaller size and weight. Industry implementations are referred to as “TSV” technology, which stands for multi-chip modules with through silicon vias (“TSV”).

On information and belief, products sold or manufactured in the United States, but by no means limited to, the Apple iPhone 6, the Apple iPhone 6 Plus, the Samsung Galaxy Tab, and the HTC 601. These and other products.
PATENT LITIGATIONS
ELM 3DS vs. Micron Technology

Case 1:14-cv-01431-UNA filed 21/11/2014
Plaintiff: ELM 3DS Innovation
Defendant: Micron Technology

IN THE UNITED STATES DISTRICT COURT FOR THE DISTRICT OF DELAWARE

Micron has infringed and continues to infringe the ELM 3DS Patents, direct semiconductor products with multiple stacked die and/or electronics products resulting there from.

The ELM 3DS Patents in-suit in ELM 3DS vs. Micron Technology case cover fundamental technologies that enable semiconductor manufacturers to form interconnect circuitry for communication among the stacked die, including circuits such as memory, processors, and image sensors. These fundamental technologies enable the ELM 3DS Patents to disclose technologies that enable semiconductor manufacturers to form interconnect circuitry for communication among the stacked die, including:

On information and belief, products sold or manufactured in the United States incorporating Micron’s infringing products are currently offered for sale in the United States. Moreover, through its marketing of the infringing stacked semiconductor products, Micron has marketed its infringing stacked semiconductor products to third parties for inclusion in DRAM products — many of which are stacked memory products — and primarily used in devices. Further, Micron has stated that its embedded NAND Flash-based storages, computers, industrial and automotive applications, networking and other products through Intel and Xilinx shows that it has specifically intended to and has induced
PATENT LITIGATIONS
ELM 3DS vs. Samsung Electronics

Case 1:14-cv-01430-UNA filed 21/11/2014
Defendant: Samsung Electronics

IN THE UNITED STATES DISTRICT COURT FOR THE DISTRICT OF DELAWARE

Samsung has infringed and continues to infringe the Elm 3DS patents, directly and indirectly, by making, using, selling, offering for sale, and importing into the United States, semiconductor products with multiple stacked die and memory modules that use the Elm 3DS patents. Elm 3DS owns the patents and is managing their patent portfolio containing the same, with knowledge of the Elm 3DS patents and in the infringing products. Samsung has done so with the knowledge that products it makes, uses, and sells in the United States infringe the Elm 3DS patents. The Elm 3DS Patents disclose three-dimensional integrated circuit structures and methods of manufacture and use. In particular, the Elm 3DS Patents disclose a three-dimensional structure with thinned and polished silicon substrates that are electrically connected. The disclosed technology enhances memory speed and reduces power consumption. The disclosed technology improves memory density because multiple storage arrays can be stacked. Such implementations are referred to as “stacked” memories that are electrically connected and used in conventional integrated circuits.

On information and belief, products sold or manufactured in the United States by Samsung include, but are not limited to, the Apple MacBook Pro, the Dell PowerEdge server, the Amazon Kindle Fire HDX 7”, the Microsoft Surface, and the Google Chromecast. These products are currently offered for sale in the United States.
<table>
<thead>
<tr>
<th>Patent Number</th>
<th>Title</th>
<th>Priority Date</th>
<th>Legal Status</th>
<th>Expected Expiration Date</th>
<th>Main Claim</th>
</tr>
</thead>
<tbody>
<tr>
<td>US8085333</td>
<td>Adjacent substantially flexible integrated circuits that are bonded by a non-conductive layer</td>
<td>03/03/2003</td>
<td>Granted</td>
<td>30/12/2018</td>
<td>Each substrate having integrated circuits, each substrate having 1st substantially planar surface; 1st thermal diffusion bonds contact between a majority of 1st surface of 3rd substrate.</td>
</tr>
<tr>
<td>US7608715</td>
<td>Three-dimensional structure memory</td>
<td>18/12/2003</td>
<td>Granted</td>
<td>11/04/2017</td>
<td>A stacked integrated circuit comprises a plurality of thinned substantially flexible integrated circuits, wherein a plurality of thinned substantially flexible integrated circuits comprises 1st substantially flexible integrated circuit wherein a plurality of 1st interconnections are located on 2nd surface, said 1st and 2nd surfaces face each other and said plurality of 2nd interconnections are substantially planar electrically coupled to form a plurality of vertical interconnections; and said plurality of thinned substantially flexible integrated circuit and the plurality of thinned substantially flexible interconnections are positioned in a stacked relation to one another, and wherein a plurality of thinned substantially flexible integrated circuits comprises a sub.</td>
</tr>
</tbody>
</table>
PATENT LITIGATIONS

Present Status of the Cases

• In 2015, Samsung Electronics Co., Ltd.; Micron Technology, Inc.; and SK Hynix Inc. (collectively, “Petitioner”) request inter partes review (“IPR”) of claims 1, 2, 4, and 49 of US8907499 (“the ‘499 patent’): IPR2016-00708, which, on its face, is assigned to Elm 3DS Innovations, LLC (“Patent Owner”). An inter partes review is used to challenge the patentability of one or more claims in a U.S. patent only on a ground that could be raised under 35 U.S.C. §§ 102 or 103, and only on the basis of prior art consisting of patents or printed publications (http://www.uspto.gov/patents-application-process/appealing-patent-decisions/trials/ipr/ipr). Patent Owner has also asserted related US7193239; US7474004; US8496862; US8982119; and US8933570 in one or more of these additional IPRs: IPR2016-00388 and IPR2016-00393; IPR2016-00394; IPR2016-00386; and IPR2016-00691. And Micron Technology, Inc. and SK Hynix Inc. have concurrently filed another IPR petition on the same patents. Petitioner is also concurrently filing another IPR petition on claims 1, 2, 4, and 49 of US8907499 (IPR2016-00706). For each of these inter partes review, Dr Paul D. Franzon submitted high-quality evidence and expert testimony in support of the petition. Before the patent trial and appeal board, petitioners respectfully unpatentable, in view of the following grounds under 35 U.S.C. § 103.

• ELM 3DS submitted many documents to reject these cancellations. (Details on the IPR can be found in the appendix; see the supporting evidence and patent cancellations.)

Details for each Inter Partes Review (IPR) are described in the next slide.

To obtain more information and follow the status of the cases: https://ptabtrials.uspto.gov
### PATENT LITIGATIONS

#### Present Status of the Inter-Partes Review (1/5)

<table>
<thead>
<tr>
<th>IPR Number</th>
<th>Filing Date</th>
<th>Patent Number</th>
<th>Challenged Claim</th>
<th>Petitioner Comments Dr Paul D. Franzon</th>
<th>ELM 3DS Comments</th>
<th>Present Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPR2016-00708 Last Notice: 8/07</td>
<td>17/03/2016</td>
<td>US8907499 ELM 3DS</td>
<td>1 &amp; 49</td>
<td>Petitioner 1 &amp; 49 not established a patentable. If the invention is not patentable then the challenged claim should not be 1 &amp; 49</td>
<td>Not established a patentable. If the invention is not patentable then the challenged claim should not be patentable.</td>
<td>Pending</td>
</tr>
<tr>
<td>IPR2016-00770 Last Notice: 8/07</td>
<td>17/03/2016</td>
<td>US8907499 ELM 3DS</td>
<td>12, 13, 24, 36, 37, 38, 53, 83, 86, 87, and 132</td>
<td>Petitioner 12, 13, 24, 36, 37, 38, 53, 83, 86, 87, and 132 not established a patentable. If the invention is not patentable then the challenged claim should not be patentable.</td>
<td>Not established a patentable. If the invention is not patentable then the challenged claim should not be patentable.</td>
<td>Pending</td>
</tr>
<tr>
<td>IPR2016-00388 Last Notice: 1/07</td>
<td>28/12/2015</td>
<td>US7193239 ELM 3DS</td>
<td>1, 10-12, 13, 18-20, 60-63, 67, 70-73, and 77</td>
<td>Petitioner 1, 10-12, 13, 18-20, 60-63, 67, 70-73, and 77 is not established a patentable. If the invention is not patentable then the challenged claim should not be patentable.</td>
<td>Pending</td>
<td></td>
</tr>
</tbody>
</table>

To obtain more information and follow the status of the cases: [https://ptabtrials.uspto.gov](https://ptabtrials.uspto.gov)
Excel Database
with all patents analyzed in the report with technology segmentation

This database allows multi-criteria searches and includes patent publication number, hyperlinks to the original documents, priority date, title, abstract, patent assignees, technological segments and legal status for each member of the patent family.
ORDER FORM

TSV Stacked Memory – Patent Landscape Analysis
September 2016

PRODUCT ORDER

<p>| | |</p>
<table>
<thead>
<tr>
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<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>€4,990</td>
<td>Single user license*</td>
</tr>
<tr>
<td>€5,990</td>
<td>Corporate license</td>
</tr>
</tbody>
</table>

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I hereby accept Knowmade’s Terms and Conditions of Sale

Signature:

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Name (Mr/Ms/Dr/Pr):

Job Title:

Company:

Address:

City:

State:

Postcode/Zip:

Country:

VAT ID Number for EU members:

Tel:

Email:

Date:

PAYMENT METHODS

Check
To pay your invoice using a check, please mail your check to the following address:

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2405 route des Dolines, BP 65
06902 Valbonne Sophia Antipolis
FRANCE

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To pay your invoice using a bank money wire transfer please contact your bank to complete this process. Here is the information that you will need to submit the payment:

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Bank: Banque populaire St Laurent du Var CAP 3000 - Quartier du lac- 06700 St Laurent du Var
IBAN: FR76 1560 7000 6360 6214 5695 126
BIC/SWIFT: CCBFRPPP

Paypal
In order to pay your invoice via PAYPAL, you must first register at www.paypal.com. Then you can send money to the KnowMade S.A.R.L. by entering our E-mail address contact@knowmade.fr as the recipient and entering the invoice amount.

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E-mail: contact@knowmade.fr
Mail: KnowMade S.A.R.L. 2405 route des Dolines, 06902 Sophia Antipolis, FRANCE

I hereby accept Knowmade’s Terms and Conditions of Sale

Signature:
DEFINITIONS

2. Acceptance: By which the Buyer accepts, the terms and conditions of sale in their entirety. It is done by signing the purchase order which mentions “I hereby accept Knowmade’s Terms and Conditions of Sale”.

3. Buyer: Any business user (i.e. anyone acting in the course of its business activities, for its business needs) entering into the following general conditions to the exclusion of consumers acting in their personal interests.

4. "Contracting Parties" or “Parties”: The Seller on the one hand and the Buyer on the other hand.

5. "Intellectual Property Rights" (“IPR”): means any rights held by the Seller in its Products, including any patents, trademarks, designs, copyrights, inventions, commercial secrets, product know-how, technical information, company or trading names and any other intellectual property rights or similar in any part of the world, which may have been registered or not and including any pending registration of one of the above mentioned rights.

6. License: For the reports and databases, 2 different licenses are proposed. The buyer has to choose one license.

1. One user license: a single individual at the company can use the report.

2. Multi-user license: the report can be used by unlimited users within the company. Subscriptions are not included.

7. Products: Reports are established in PowerPoint and delivered on a PDF format and the database may include Excel files.

8. Seller: Based in Sophia Antipolis (France headquarters), Knowmade is a technology intelligence company specialized in the identification and analysis of technical landscapes and scientific state of the art with high added value to businesses and research laboratories. Our intelligencedigests play a key role to define your innovation and development strategy.

1. SCOPE

4.1. The Contracting Parties undertake to observe the following general conditions when agreed by the Buyer and the Seller. ANY ADDITIONAL, DIFFERENT, OR CONFLICTING TERMS AND CONDITIONS IN ANY OTHER DOCUMENTS ISSUED BY THE BUYER AT ANY TIME ARE HEREBY OBSCURED TO BE DISREGARDED BY THE SELLER, SHALL BE WHOLLY INAPPLICABLE TO ANY SALE MADE HEREBEIN AND SHALL NOT BE Binding IN ANY WAY ON THE SELLER.

4.2. This agreement becomes valid and enforceable between the Contracting Parties after clear and non- equivocal consent by any duly authorized person representing the Buyer. For these purposes, the Buyer accepts to be informed about the terms and conditions of this Agreement, defined by Knowmade’s Terms and Conditions of Sale”. This results in acceptance by the Buyer.

4.3. The Buyer is deemed to be accepted only upon written acceptance and confirmation by the Seller, within 7 days from the date of order, to be sent either by email or to the Buyer’s address. In the absence of any confirmation in writing, orders shall be deemed to have been accepted.

2. MAILINGS OF THE PRODUCTS

4.1. Products are sent by mail to the Buyer:

1. within [1] month from the order for Products already released; or

2. within a reasonable time for Products ordered prior to their effective release. In this case, the Seller shall use its best efforts to inform the Buyer of an indicative release date and the evolution of the work in progress.

2.1. some weeks prior to the release date the Seller can propose a pre-release discount to the Buyer.

2.2. The Seller shall by no means be responsible for any delay in respect of article 2.2 above, and including in cases where a new event or access to new contradictory information would require for the analyst extra time to compute or compare the data in order to enable the Seller to deliver a high quality Product.

2.3. The mailing of the Product will occur only upon payment by the Buyer, in accordance with the conditions contained in article 5.1.

2.4. The mailing is operated through electronic means either by email via the sales department. If the Product’s electronic format is defective, the Seller undertakes to replace it at no charge to the Buyer provided that it is informed of the defective formatting within 90 days from the date of the original download or receipt of the Product.

2.5. The person receiving the Products on behalf of the Buyer shall immediately verify the quality of the Products and their conformity to the order. Any claim for apparent defects or non-conformity shall be sent in writing to the Seller within 8 days of receipt of the Products. For this purpose, the Buyer agrees to produce sufficient evidence of such defects.

3. PRICE, INVOICING AND PAYMENT

3.1. Prices are given in the orders corresponding to each Product sold on a unit basis or corresponding to annual subscriptions. They are expressed to be inclusive of all taxes. The prices may be reevaluated from time to time by the Seller on the basis of any applicable tax changes and shall be notified to the Buyer in the time of the order.

3.2. Payments due by the Buyer shall be sent by cheque payable to Knowmade, PayPal or by electronic transfer to the account of the Seller indicated in the purchase order or in the invoice. The Buyer will be informed of the Seller’s account number by means of a bank requisition, and other payments shall be made by means of a bank requisition to: Banque populate St- Laurent du Var CAP 3000 - Quartier du lac: 06700 St Laurent du Var BIC or SWIFT code: CCBF8880

3.3. In case of late payment, this will be charged an interest rate of 10% per annum on the late payment amount, calculated on the basis of the annual rate Ref of the «ECE» + 5 points, in accordance with article L. 441-6 of the French Commercial Code. Our publications (report, database, tool...) are sold only if a paid order is sent to our Head Office.

3.4. In the event of termination of the contract, or of misconduct, during the contract, the Seller will have the right to invoice at the stage in progress, and to take legal action for damages.

4. LIABILITIES

4.1. Compensation or any other individual or legal person acting on its behalf, being a business user buying the Products for its business activities, shall be solely responsible for choosing the Products and for the use and interpretations he makes of the documents it purchases, of the results he obtains, and of the advice and acts it deduced thereof.

4.2. The Seller shall only be liable for (i) direct and (ii) foreseeable pecuniary loss, caused by the Products or any event as a result of this agreement.

4.3. In no event shall the Seller be liable for:

a) any indirect, special, incidental, consequential or damages (including, but not limited to, damages for loss of profits, business interruption and loss of programs or information) arising out of the use or inability to use the Seller’s website or the Products, or any information provided on the website, or on a related board (in the event an online product is offered);

b) any claim attributable to errors, omissions or other inaccuracies in the Product or interpretations thereof through the use of the Product;

c) All the information contained in the Products has been obtained from sources believed to be reliable. The Seller does not warrant the accuracy, completeness adequacy or reliability of such information, which is provided "as is" and without warranty or representation of any kind.

4.5. All the Products that the Seller sells may, upon prior notice to the Buyer from time to time be modified or updated in response to the needs of the Buyer. This modification shall not lead to the liability of the Seller, provided that the Seller ensures the substituted Product is similar to the Product initially ordered.

4.6. In the case where, after inspection, it is acknowledged that the Products contain defects, the Seller undertakes to replace the defective products as far as the supplies allow and without indemnities or compensation of any kind for labor costs, delays, loss or any other reason. The replacement is guaranteed for a maximum of 2 months starting from the delivery date. Any replacement is excluded for unforeseeable reasons.

4.7. The deadlines that the Seller is asked to state for the mailing of the Products are given for information only and are not guaranteed. If such deadlines are not met, it shall not lead to any damages or cancellation of the order. Any delay from the date of order, as an исключительное право, will not result in any new information from the Seller. In such case only, the Buyer shall be entitled to ask for a reimbursement of its first down payment in the exclusion of any further damages.

4.8. The Seller does not make any warranties, express or implied, including, without limitation, those of saleability and fitness for a particular purpose, with respect to the Products. Although the Seller shall take reasonable steps to screen Products for infection of viruses, worms, Trojan horses or other codes that might harm the end-user or the operation of the Buyer’s computer systems, the Buyer shall be fully responsible for conducting its own due diligence to ascertain the fitness of the Product for its purposes.

5. FORCE MAJEURE

5.1. The Seller shall not be liable for any delay in performance directly or indirectly caused by or resulting from acts of nature, fire, flood, accident, riot, war, government intervention, embargoes, strikes, epidemics, difficulties, equipment failure, late deliveries by suppliers or other difficulties which are beyond the control of the Seller and which were not foreseeable by the Seller.

6. PROTECTION OF THE SELLER’S IPR

6.1. All the IPR attached to the Products and are the property of the Seller and are protected under French and international copyright law and conventions.

6.2. The Buyer agreed not to disclose, copy, reproduce, redistribute, resell or publish the Product, or any part of it to any other party other than employees of its company. The Buyer shall have the right to use the Product for its own use and for its internal use only for the purposes indicated in the IPR.

6.3. The Buyer shall be solely responsible to the Seller of all infringements of this obligation, whether this infringement comes from its employees or any person to whom the Buyer has sent the Products and shall personally take care of any related proceedings, and the Buyer shall bear related financial consequences in their entirety.

6.4. The Buyer shall define within its company point of contact for the needs of the contract. This person will be the recipient of each new report in PDF format. This person shall also be responsible for the respect of the copyrights and will guaranty that the Products are not disseminated out of the company.

7. TERMINATION

7.1. If the Buyer cancels the order in whole or in part or postpones the date of mailing, the Buyer shall be entitled to request a proportional refund of the products. The Seller shall have the exclusive right to decide upon the validity of such delay or cancellation. This may also apply for any other direct or indirect consequential loss that may be borne by the Seller, following this decision.

7.2. In the event of breach by one Party under these conditions or the order, the non-breaching Party may send a notification to the other by recorded delivery letter upon which, after a period of thirty (30) days without solving the problem, the non-breaching Party shall be entitled to terminate all the pending orders, without being liable for any compensation.

8. MISCELLANEOUS

8.1. All the provisions of these Terms and Conditions are for the benefit of the Seller itself, but also for its agents, its employees, its suppliers and agents. Each of them is entitled to assert and enforce those provisions against the Buyer.

8.2. Any waivers or modifications to these Terms and Conditions shall be given in writing. They shall be effective upon receipt by the other Party. The Seller may, from time to time, update these Terms and Conditions and the Buyer, is deemed to have accepted the latest version of these terms and conditions, provided they have been communicated to him in due time.

9. GOVERNING LAW AND JURISDICTION

9.1. Any dispute arising out of or linked to these Terms and Conditions or to any contract (order) executed into this Agreement and concerning any matter connected with the implementation or interpretation of the same, shall have exclusive jurisdiction upon such issues.

9.2. The Buyer shall not govern the relation between the Buyer and the Seller, in accordance with these Terms and Conditions.